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SPECIFICATION

METHOD FOR REDUCING NOISE IN INTEGRATED CIRCUIT LAYOUTS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates noise problems in integrated circuits. More particularly, the present invention provides a method for inserting buffers into an integrated circuit layout during the place and route stage in order to reduce the overall noise introduced into conductive paths in a given design.

2. The Background Art

As the speed of signals within integrated circuits increases and the distance between conductive paths decreases, the problem of reducing the susceptibility of conductive paths to noise becomes increasingly important.

In the prior art conversion process between design and layout for integrated circuit systems, there are four major steps which are accomplished by system designers. Those four major steps include place and route of the standard cell design, physical design verification to ensure consistency between the layout and the schematic, parisitic extraction of the interconnect, and analysis of the extracted data to generate a noise analysis report.

When correcting the physical circuit layout in a prior art conversion process, a designer typically must either manually move wires and circuits in order to minimize or eliminate those noise problems, or may instead increase the size of the driver supplying signals to a conductive path which is deemed to be noise sensitive.

This manual process is extremely time–consuming and very tedious because by moving conductive paths or increasing drivers is likely to cause new noise problems. Those new noise problems must then be corrected, potentially causing yet a third set of noise problems. Thus, manually correcting a circuit layout in order to solve noise problems often requires considerable effort and several very time–consuming iterations.

It would therefore be beneficial to provide a method for automatically determining potentially noisy areas within circuit layouts at the place and route stage, and for correcting problems related to areas of specific concern.

SUMMARY OF THE INVENTION

A method for minimizing noise in an integrated circuit is described, the method including choosing a net to be analyzed, determining that the total path length of conductive paths coupled to a driver within the net exceeds a maximum acceptable length for that driver according to the minimum acceptable noise levels for that given net, and inserting at least one buffer within the net at a position

which is within the maximum acceptable length for conductive paths coupled to the driver.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a prior art physical circuit layout having potential noise problems.

FIG. 2 shows a prior art curve of noise amplitude vs. conductive path length.

FIG. 3 is a flowchart depicting a method of the present invention.

FIG. 4 shows the example of FIG. 1 after having placed buffers according to a method of the present invention.

DETAILED DESCRIPTION OF ONE EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons who are familiar with this disclosure.

The present invention provides a method for correcting potentially noisy circuit layouts at the place and route stage during the process of converting an electronic design into a physical circuit layout.

FIG. 1 is a block diagram of a prior art physical circuit layout having potential noise problems.

SUB A3 Referring to FIG. 1, layout 10 includes driver/receivers 12 and 14 coupled together using conductive path 16. Further included are driver/receivers 18 and 20, driver 22 and receiver 24. Driver/receiver 18 is coupled to driver/receiver 20 using conductive path segments 26 and 28. At the intersection of conductive path segments 26 and 28, a conductive path segment 30 is coupled thereto. Driver 22 and receiver 24 are coupled to conductive path segments 32 and 34 respectively. Conductive path segments 32 and 34 are further coupled to conductive path segment 30.

SUB A4 The present invention analyzes each net individually to determine whether a given net is likely to have more than an acceptable level of noise coupled to it from external sources. External sources are considered to be anything other than net components such as driver/receiver combinations or drivers or receivers individually.

SUB A5 Although the coupling capacitance between interconnects is a source of potential coupling noise problems, the symptom of the noise peak is demonstrated

at the output of the receiving cell. Different CMOS cells have differing tolerance for coupling noise impinging on their inputs. The choice for the maximum allowable wire length for noice violations to be prevented is therefore not only dependant on the strength of the victim and aggressor drivers, but also on the type of cell at the end of the victim interconnect.

The present invention noise analysis is performed using well-known curves for various driver circuits of noise amplitude vs. the length of a conductive path coupled to that driver circuit. It is well-known that a conductive path of a given length being driven by a weak driver will have a higher susceptibility to noise than that same conductive path when driven by a stronger driver.

For each conductive path, there is a given amount of noise that can be tolerated, depending on what signals on that conductive path are accomplishing. It is up to the circuit designer to determine what the acceptable levels of noise will be on the various types of conductive paths being used in a given design. Such an acceptable level might be pictorially represented as line 40 in FIG. 2. The point at which line 40 intersects with a driver noise amplitude line determines the maximum length of conductive path that may be between a driver in the receiver without any intervening circuitry such as buffers or other circuits.

SUB A7 FIG. 3 is a flowchart depicting a method of the present invention.

Referring to FIG. 3, the method begins at block 50 where a net is chosen for analysis. It is contemplated that all critical nets in a given design will be analyzed. However, not all nets in every design will necessarily be analyzed according to the present invention.

SUB A7 At block 52, using the noisy amplitude vs. distance data which is known by those of ordinary skill in the art and the acceptable noise levels previously determined for that given circuit type, it is determined whether the net chosen at block 50 is likely to exceed the acceptable noise levels. That question is posed a block 54, and if the chosen net is likely to exceed maximum acceptable noise levels, it is determined, at block 56, whether a larger driver is available in the driver library which would solve the problem. If so, the method proceeds at block 58 where a larger driver is chosen to replace the previously determined weaker driver, thus solving the noise problem for this net.

An example of a larger driver solving the problem is seen in FIG. 2 where, in this example, the driver having the characteristics shown by curve 58 might have been originally chosen for the physical layout. Suppose in this example, point 60 on curve 58 represents the length of the conductive path being analyzed. It is easily seen that point 60 is above the acceptable noise level line 40. However, curves 62 and 64, representing stronger drivers, for the same length of conductive path would result in acceptable noise levels as represented by points 66 and 68 respectively.

If, at step 56, a larger driver was not available, the method proceeds at block 70 where a buffer is placed at a location which would increase signal levels on the net. Locations where drivers are placed may be thought to be locations where the previous net ends and a new net begins. Thus, a buffer is placed at a location which would cause the conductive path between the driver and the buffer to be shorter than would otherwise have occurred. Since the conductive path is shorter, there is less susceptibility to noise.

In order to properly place a buffer so as to minimize the noise in a given net, it is necessary to know the point at which acceptable noise level line 40 and FIG. 2 crosses the curve for the given driver. Thus, if a driver is employed which is represented by curve 62, it is necessary to know where point 72 is located. Knowing where point 72 is located gives you the maximum length of conductive path allowed in order to achieve an acceptable noise level for that conductive path.

When determining where to place a buffer, it is important to recognize that a conductive path includes all conductive path segments leaving a given driver, including all intersecting paths. Using the example of FIG. 1, the total length of conductive path segments between driver/receiver 18 and point 72 on conductive path segment 30 includes all of conductive path segment 26, all of conductive path segment 28, and that portion of conductive path 30 between point 72 and intersection point 74.

FIG. 4 shows the example of FIG. 1 after having placed buffers according to the method of the present invention.

Referring to FIG. 4, the net which includes driver/receiver 12, driver/receiver 14, and conductive path 16 has not been duplicated because it was previously determined that this net resulted in acceptable noise levels. The remaining net includes driver/receiver 18 and receiver 24 from FIG. 1, new driver/receiver 80, and new driver 82.

Assume now that it is time to analyze driver/receiver 18 and the conductive paths coupled thereto. Using the curve associated with driver/receiver 18, a given maximum length for conductive paths coupled to driver/receiver 18 will be known because the maximum acceptable length for those conductive paths will have been determined by knowing the maximum acceptable noise level allowed on those conductive paths.

Assume that the various lengths of conductive path segments 84, 86, 88, and 90 add up to the maximum acceptable length for a conductive path coupled to driver/receiver 18. It is acceptable then, to provide a buffer at any point on conductive paths 84, 86, 88, or 90.

It is most desirable at this point, to determine if there are timing issues with respect to driver/receiver 18 and/or driver/receiver 80 which would make it more desirable to place a buffer in either conductive path segment 84 or either of conductive path segments 88 or 90. If it is critical that signals being transmitted

from driver/receiver 80 travel more quickly over the various conductive paths to, for example, receiver 24, it would be more beneficial to place a required buffer within conductive path 84, rather than, for example, within conductive path 86.

SUB A2 Now assume that buffer 92 has been placed within conductive path 84 because it is necessary that signals from driver/receiver 80 arrive at receiver 24 as quickly as possible. Once buffer 92 has been placed, the new question becomes whether the total conductive path length between the output of driver 92 and the input to receiver 24 meets the previously defined criteria for noise.

SUB A3 If the previously defined criteria for noise is not met by the remaining total conductive path length, is again necessary, at block 96 of FIG. 3, to determine where to place another buffer. Now, the FIG. 2 curve to be used is that curve associated with buffer 92. A new maximum acceptable path length will be determined from that curve, and it may be necessary to add a second buffer such as buffer 96.

Those of ordinary skill in the art having the benefit of this disclosure would readily recognize that the methods described herein may easily be incorporated in place and route software. It is also contemplated that the methods described herein may be incorporated into a state machine or other application–specific integrated circuits.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.